PC16550D Universal Asynchronous Receiver/Transmitter With FIFOs

1 Features

- Capable of Running All Existing 16450 Software.
- Pin for Pin Compatible With the Existing 16450 Except for CSOUT (24) and NC (29). The Former CSOUT and NC Pins Are $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$, Respectively.
- After Reset, All Registers Are Identical to the 16450 Register Set.
- In the FIFO[(1)] Mode Transmitter and Receiver Are Each Buffered With 16 Byte FIFO's to Reduce the Number of Interrupts Presented to the CPU.
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or From the Serial Data.
- Holding and Shift Registers in the 16450 Mode Eliminate the Need for Precise Synchronization Between the CPU and Serial Data.
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts.
- Programmable Baud Generator Divides Any Input Clock by 1 to (2^{16} – 1) and Generates the 16 × Clock.
- Independent Receiver Clock Input.
- MODEM Control Functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully Programmable Serial-Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud Generation (DC to 1.5 M Baud).
- False Start Bit Detection.
- Complete Status Reporting Capabilities.
- TRI-STATE TTL Drive for the Data and Control Buses.
- Line Break Generation and Detection.
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation.
- Full Prioritized Interrupt System Controls.

2 Applications

Modems or Generic UART Communication

(1) This part is patented

3 Description

The PC16550D device is an improved version of the original 16450 Universal Asynchronous Receiver/Transmitter (UART). Functionally identical to the 16450 on powerup (CHARACTER mode: can also be reset to 16450 Mode under software control) the PC16550D can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive software overhead.

In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two pin functions have been changed to allow signalling of DMA transfers.

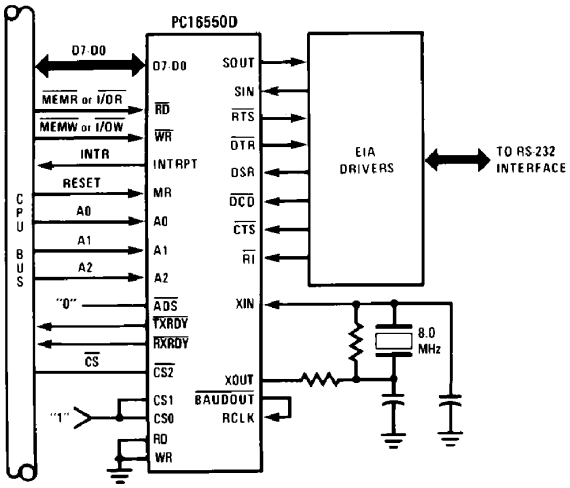
The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PC16550D	PLCC (44)	17.53 mm x 17.53 mm
	PDIP (40)	52.58 mm x 13.97 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Basic Configuration



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (continued) ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 8
7.1 Absolute Maximum Ratings ... 8
7.2 ESD Ratings ... 8
7.3 Recommended Operating Conditions ... 8
7.4 Electrical Characteristics ... 8
7.5 Timing Requirements ... 9
8 Detailed Description ... 15
8.1 Overview ... 15
8.2 Functional Block Diagram ... 15
8.3 Feature Description ... 16
8.4 Device Functional Modes ... 16
8.5 Programming ... 17
8.6 Register Maps ... 17
9 Application and Implementation ... 25
9.1 Application Information ... 25
9.2 Typical Applications ... 25
9.3 System Examples ... 27
10 Power Supply Recommendations ... 27
11 Layout ... 27
11.1 Layout Guidelines ... 27
12 Device and Documentation Support ... 28
12.1 Community Resources ... 28
12.2 Trademarks ... 28
12.3 Electrostatic Discharge Caution ... 28
12.4 Glossary ... 28
13 Mechanical, Packaging, and Orderable Information ... 28

4 Revision History

Changes from Revision B (June 1995) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted the TQFP Package drawing	3

Copyright © 1995–2015, Texas Instruments Incorporated

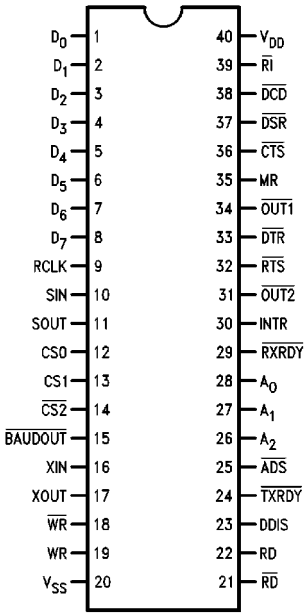
5 Description (continued)

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}–1), and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

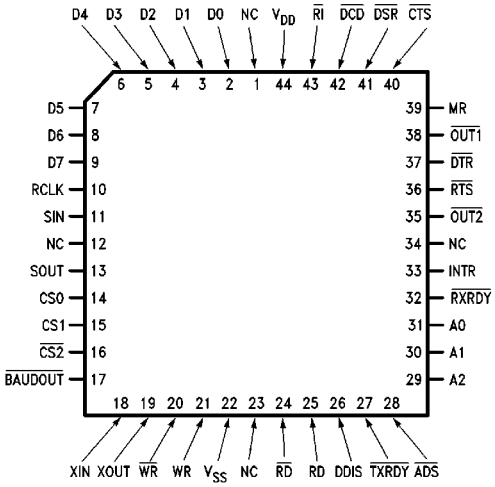
The UART is fabricated using Texas Instruments advanced M^2CMOS process.

6 Pin Configuration and Functions

NFJ Package
44-Pin PDIP
Top View



FN Package
44-Pin PLCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION (1)
NAME	PDIP	PLCC		
A0	28	31	I	Register Select. Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.
A1	27	30	I	
A2	26	29	I	
$\overline{ADS}$	25	28	I	Address Strobe. The positive edge of an active Address Strobe ($\overline{ADS}$) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals. **NOTE** An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.
$\overline{BAUDOUT}$	15	17	O	Baud Out. This is the 16 × clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.
CS0	12	14	I	Chip Select. When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the t_{CSW} parameter.
CS1	13	15	I	
CS2	14	16	I	
D_0	1	2	I/O	Data Bus. This bus comprises eight TRISTATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred through the D_7–D_0 Data Bus.
D_1	2	3	I/O	
D_2	3	4	I/O	
D_3	4	5	I/O	
D_4	5	6	I/O	
D_5	6	7	I/O	
D_6	7	8	I/O	
D_7	8	9	I/O	
$\overline{CTS}$	36	40	I	Clear to Send. When low, this indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. **NOTE** Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

(1) The following describes the function of all UART pins. Some of these descriptions reference internal circuits. In the following descriptions, a low represents a logic 0 (0 V nominal) and a high represents a logic 1 (2.4 V nominal).

Copyright © 1995–2015, Texas Instruments Incorporated

Pin Functions (continued)

PIN			I/O	DESCRIPTION[1]
NAME	PDIP	PLCC		
$\overline{DCD}$	38	42	I	Data Carrier Detect. When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. **NOTE** Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
DDIS	23	26	O	Driver Disable. This goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART.
DSR	37	41	I	Data Set Ready. When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. **NOTE** Whenever the DDSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{DTR}$	33	37	O	Data Terminal Ready. When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
INTR	30	33	O	Interrupt. This pin goes high whenever any one of the following interrupt types has an active high condition and is enabled through the IER Receiver Error Flag; Received Data Available timeout (FIFO Mode only); Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.
MR	35	39	I	Master Reset. When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input (Refer to Table 3) This input is buffered with a TTL-compatible Schmitt Trigger with 0.5-V typical hysteresis.
$\overline{OUT\ 1}$	34	38	O	Output 1. This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.
$\overline{OUT\ 2}$	31	35	O	Output 2. This user-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.
RCLK	9	10	I	Receiver Clock. This input is the 16 x baud rate clock for the receiver section of the chip.
RD	22	25	I	Read. When RD is high or $\overline{RD}$ is low while the chip is selected, the CPU can read status information or data from the selected UART register. **NOTE** Only an active RD or RD input is required to transfer data from the UART during a read operation. Therefore, tie either the RD input permanently low or the RD input permanently high, when it is not used.
$\overline{RD}$	21	24	I	

Pin Functions (continued)

PIN			I/O	DESCRIPTION(1)
NAME	PDIP	PLCC		
$\overline{RI}$	39	43	I	Ring Indicator. When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input **signal** has changed from a low to a high state since the previous reading of the MODEM Status Register. **NOTE** Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{RTS}$	32	36	O	Request to Send. When low, this informs the MODEM or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{RXRDY}$	29	32	O	Receiver. DMA signaling is available through two pins (24 and 29). When operating in the FIFO mode, one of two types of DMA signaling per pin can be selected through FCR3. When operating as in the 16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied or the XMIT FIFO has been filled. **Mode 0**: When in the 16450 Mode (FCR0e0) or in the FIFO Mode (FCR0=1, FCR3=0) and there is at least 1 character in the RCVR FIFO or RCVR holding register, the RXRDY pin (29) will be low active. Once it is activated the RXRDY pin will go inactive when there are no more characters in the FIFO or holding register. **Mode 1**: In the FIFO Mode (FCR0=1) when the FCR3=1 and the trigger level or the timeout has been reached, the RXRDY pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or holding register.
SIN	10	11	I	Serial Input. Serial data input from the communications link (peripheral device, MODEM, or data set).
SOUT	11	13	O	Serial Output. Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.
$\overline{TXRDY}$	24	27	O	Transmitter. DMA signaling is available through two pins (24 and 29). When operating in the FIFO mode, one of two types of DMA signaling per pin can be selected through FCR3. When operating as in the 16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied or the XMIT FIFO has been filled. **Mode 0**: In the 16450 Mode (FCR0=0) or in the FIFO Mode (FCR0=1, FCR3=0) and there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY pin (24) will be low active. Once it is activated the TXRDY pin will go inactive after the first character is loaded into the XMIT FIFO or holding register. **Mode 1:** In the FIFO Mode (FCR0=1) when FCR3=1 and there are no characters in the XMIT FIFO, the $\overline{TXRDY}$ pin will go low active. This pin will become inactive when the XMIT FIFO is completely full.
V_{DD}	40	44	—	5-V supply.
V_{SS}	20	22	—	Ground (0 V) reference.
WR	19	21	I	Write. When WR is high or $\overline{WR}$ is low while the chip is selected, the CPU can write control words or data into the selected UART register. **NOTE** Only an active WR or $\overline{WR}$ input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the WR input permanently high, when it is not used.
$\overline{WR}$	18	20	I	
XIN	16	18	I	(External Crystal Input). This signal input is used in conjunction with XOUT to form a feedback circuit for the baud rate generator's oscillator. If a clock signal will be generated off-chip, then it should drive the baud rate generator through this pin.

Copyright © 1995–2015, Texas Instruments Incorporated

Pin Functions (continued)

PIN			I/O	DESCRIPTION[1]
NAME	PDIP	PLCC		
XOUT	17	19	O	(External Crystal Output). This signal output is used in conjunction with XIN to form a feedback circuit for the baud rate generator's oscillator. If the clock signal will be generated off-chip, then this pin is unused.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
All input or output voltages with respect to V_{SS}	–0.5	7	V
Power Dissipation		1	W
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	0	25	70	°C
V_{DD}	Supply Voltage	4.5	5	5.5	V

7.4 Electrical Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ILX}	Clock input low voltage		–0.5		0.8	V
V_{IHX}	Clock input high voltage		2.0		V_{DD}	V
V_{IL}	Input low voltage		–0.5		0.8	V
V_{IH}	Input high voltage		2		V_{DD}	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA on all (1)			0.4	V
V_{OH}	Output high voltage	I_{OH} = –1.0 mA (1)	2.4			V
I_{CC}(AV)	Average power supply current	V_{DD} = 5.5 V, T_A = 25°C, No Loads on output, SIN, DSR, DCD, CTS, RI = 2.0 V, All other inputs = 0.8 V			15	mA
I_{IL}	Input leakage	V_{DD} = 5.5 V, V_{SS} = 0 V, All other pins floating, V_{IN} = 0 V, 5.5 V			±10	mA
I_{CL}	Clock leakage				±10	mA
I_{OZ}	TRI-STATE leakage	V_{DD} = 5.5 V, V_{SS} = 0 V, V_{OUT} = 0 V, 5.25 V 1) Chip deselected 2) WRITE mode, chip selected			±20	mA
V_{ILMR}	MR Schmitt V_{IL}				0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2			V
CAPACITANCE: T_A = 25°C, V_{DD} = V_{SS} = 0 V						
C_{XIN}	Clock input capacitance	f_c = 1 MHz, Unmeasured pins returned to V_{SS}		7	9	pF
C_{XOUT}	Clock output capacitance			7	9	pF
C_{IN}	Input capacitance			5	7	pF
C_{OUT}	Output capacitance			6	8	pF
$C_{I/O}$	Input/Output capacitance			10	12	pF

(1) Does not apply to XOUT.

Copyright © 1995–2015, Texas Instruments Incorporated

7.5 Timing Requirements

T_A = 0°C to 70C, V_{DD} = 5 V ± 10%

			MIN	MAX	UNIT
t_{ADS}	Address strobe width		60		ns
t_{AH}	Address hold time		0		ns
t_{AR}	$\overline{RD}$, RD delay from address	See (1)	30		ns
t_{AS}	Address setup time		60		ns
t_{AW}	$\overline{WR}$, WR delay from address	See (1)	30		ns
t_{CH}	Chip select hold time		0		ns
t_{CS}	Chip select setup time		60		ns
t_{CSR}	$\overline{RD}$, RD delay from chip select	See (1)	30		ns
t_{CSW}	$\overline{WR}$, WR delay from select	See (1)	30		ns
t_{DH}	Data hold time		30		ns
t_{DS}	Data setup time		30		ns
t_{HZ}	$\overline{RD}$, RD to floating data delay	At 100 pF loading (2)	0	100	ns
t_{MR}	Master reset pulse width		5000		ns
t_{RA}	Address hold time from $\overline{RD}$, RD	See (1)	20		ns
t_{RC}	Read cycle delay		125		ns
t_{RCS}	Chip select hold time from $\overline{RD}$, RD	See (1)	20		ns
t_{RD}	$\overline{RD}$, RD strobe width		125		ns
t_{RDD}	$\overline{RD}$, RD to driver enable/disable	At 100 pF loading (2)		60	ns
t_{RVD}	Delay from $\overline{RD}$, RD to data	At 100 pF loading		60	ns
t_{WA}	Address hold time from $\overline{WR}$, WR	See (1)	20		ns
t_{WC}	Write cycle delay		150		ns
t_{WCS}	Chip select hold time from $\overline{WR}$, WR	See (1)	20		ns
t_{WR}	$\overline{WR}$, WR strobe width		100		ns
t_{XH}	Duration of clock high pulse	External Clock (8, Max.)	55		ns
t_{XL}	Duration of clock low pulse	External Clock (8, Max.)	55		ns
RC	Read cycle = $t_{AR} + t_{RD} + t_{RC}$		280		ns
WC	Write cycle = $t_{AW} + t_{WR} + t_{WC}$		280		ns
BAUD GENERATOR					
N	Baud divisor		1	2^{16}–1	
t_{BHD}	Baud output positive edge delay	100-pF Load		175	ns
t_{BLD}	Baud output negative edge delay	100-pF Load		175	ns
t_{HW}	Baud output up time	f_X = 8, ÷2, 100-pF Load	75		ns
t_{LW}	Baud output down time	f_X = 8, ÷2, 100-pF Load	100		ns
RECEIVER					
t_{RAI}	Delay from active edge of $\overline{RD}$ to Reset Interrupt				
				–	ns
t_{RINT}	Delay from $\overline{RD}$, RD (RD RBR/or RD LSR) to Reset Interrupt	100-pF Load		1000	ns
t_{RXI}	Delay from $\overline{RD}$ RBR to RXRDY Inactive			290	ns
t_{SCD}	Delay from RCLK to sample time			2000	ns
t_{SINT}	Delay from Stop to Set Interrupt	See (3)		1	RCLK Cycles

(1) Applicable only when $\overline{ADS}$ is tied low.
(2) Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.
(3) In the FIFO mode (FCR0=1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

Copyright © 1995–2015, Texas Instruments Incorporated

Timing Requirements (continued)

T_A = 0°C to 70C, V_{DD} = 5 V ± 10%

			MIN	MAX	UNIT
TRANSMITTER					
t_{HR}	Delay from $\overline{WR}$, WR (WR THR) to Reset Interrupt	100-pF Load		175	ns
t_{IR}	Delay from $\overline{RD}$, RD (RD IIR) to Reset Interrupt (THRE)	100-pF Load		250	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt	See (4)	16	24	BAUDOUT Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)	See (2)	8	8	BAUDOUT Cycles
t_{SXA}	Delay from Start to TXRDY active	100-pF Load		8	BAUDOUT Cycles
t_{WXI}	Delay from Write to TXRDY inactive	100-pF Load		195	ns
MODEM CONTROL					
t_{MDO}	Delay from $\overline{WR}$, WR (WR MCR) to Output	100-pF Load		200	ns
t_{RIM}	Delay from $\overline{RD}$, RD to Reset Interrupt (RD MSR)	100-pF Load		250	ns
t_{SIM}	Delay from MODEM input to set interrupt	100-pF Load		250	ns

(4) This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active. (See *FIFO Interrupt Mode Operation*).

All timings are referenced to valid 0 and valid 1.

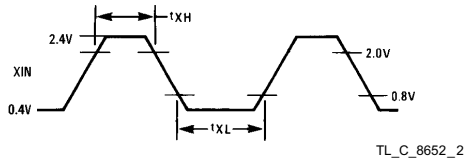


Figure 1. External Clock Input (24 MHz Max)

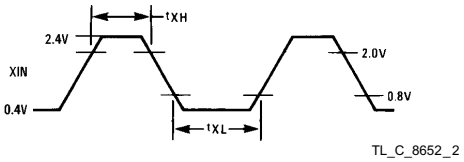


Figure 2. AC Test Points

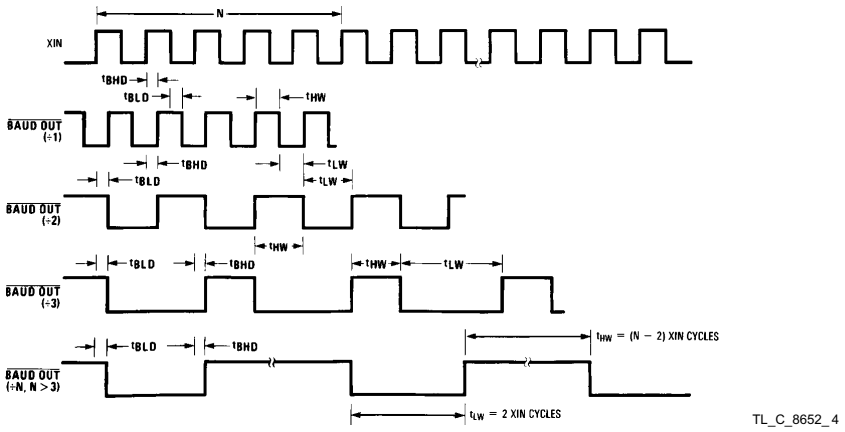


Figure 3. $\overline{BAUDOUT}$ Timing

Copyright © 1995–2015, Texas Instruments Incorporated

All timings are referenced to valid 0 and valid 1.

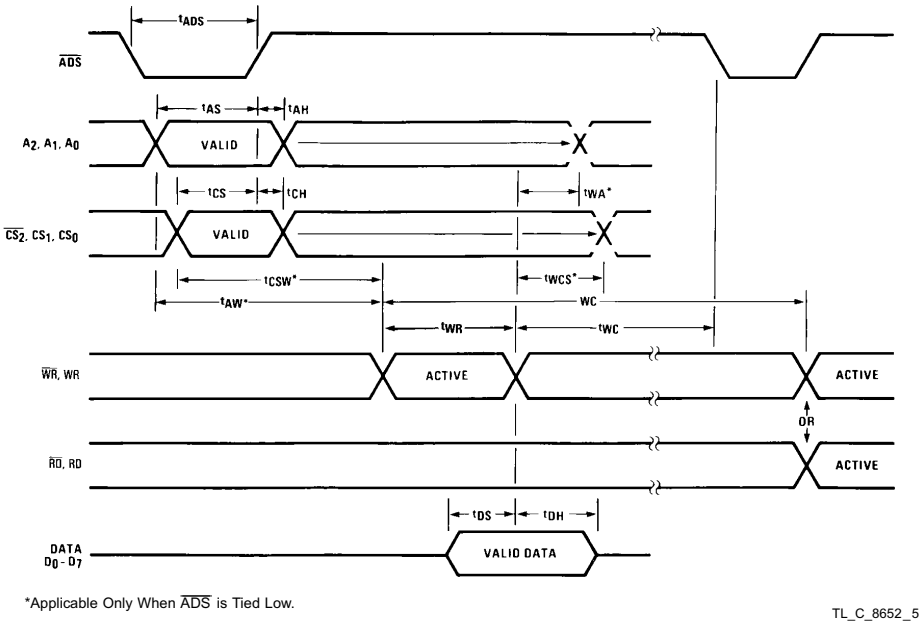


Figure 4. Write Cycle

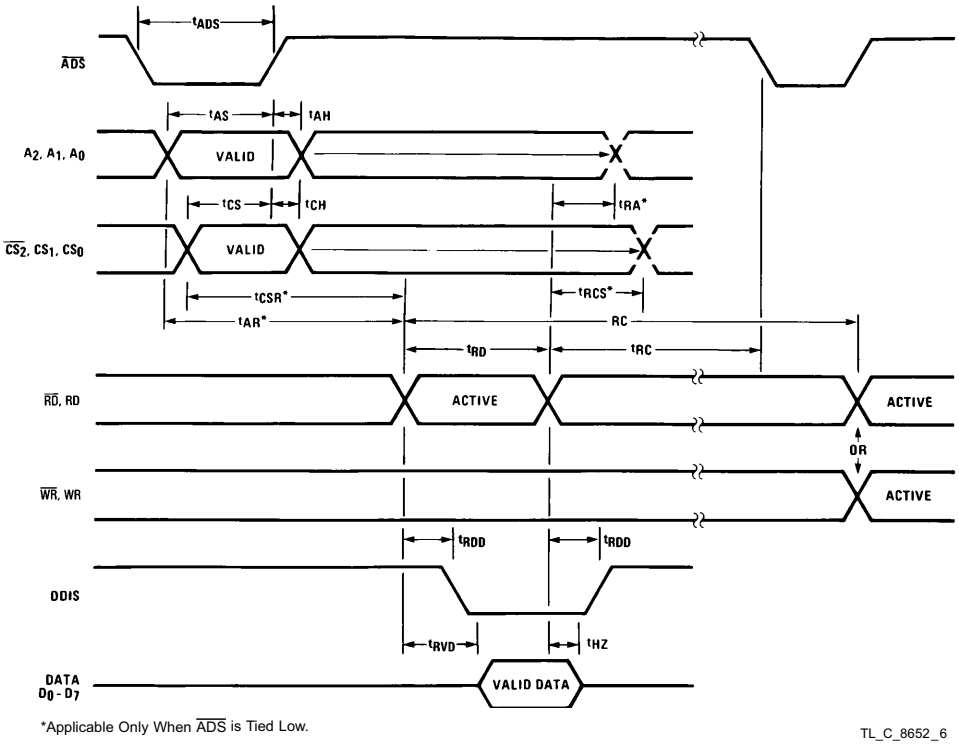


Figure 5. Read Cycle

All timings are referenced to valid 0 and valid 1.

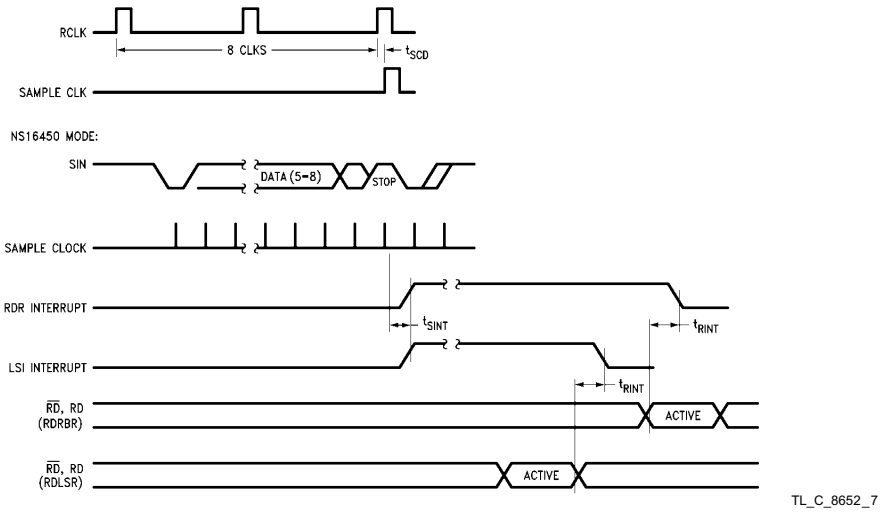


Figure 6. Receiver Timing

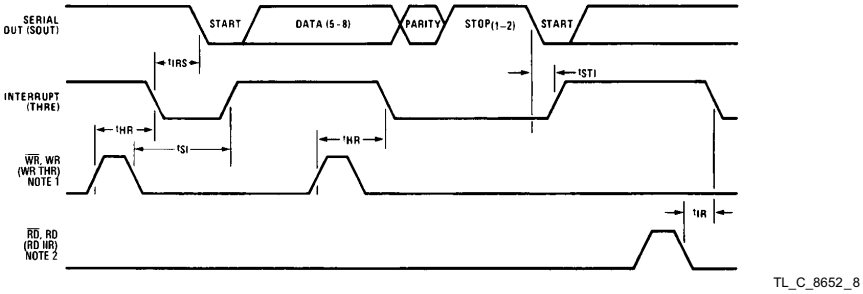
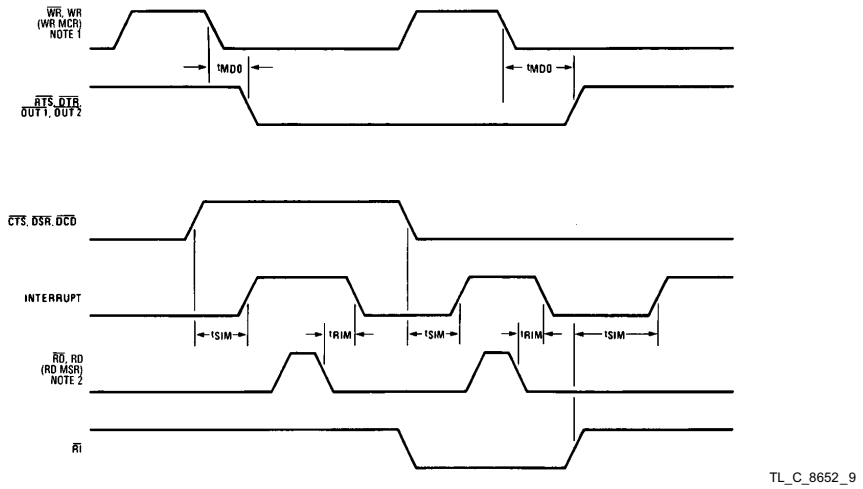


Figure 7. Transmitter Timing



(1) See Write Cycle Timing
(2) See Read Cycle Timing

Figure 8. MODEM Control Timing

Copyright © 1995–2015, Texas Instruments Incorporated

All timings are referenced to valid 0 and valid 1.

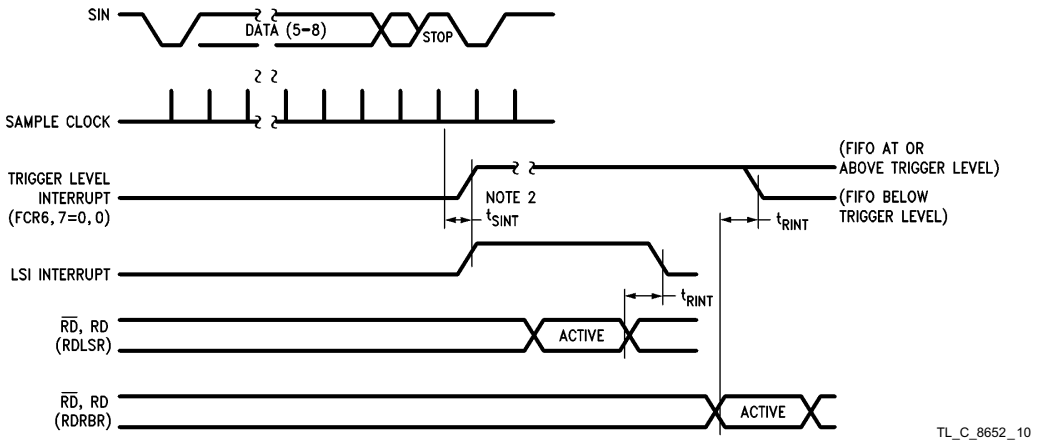


Figure 9. RCVR FIFO First Byte (This Sets RDR)

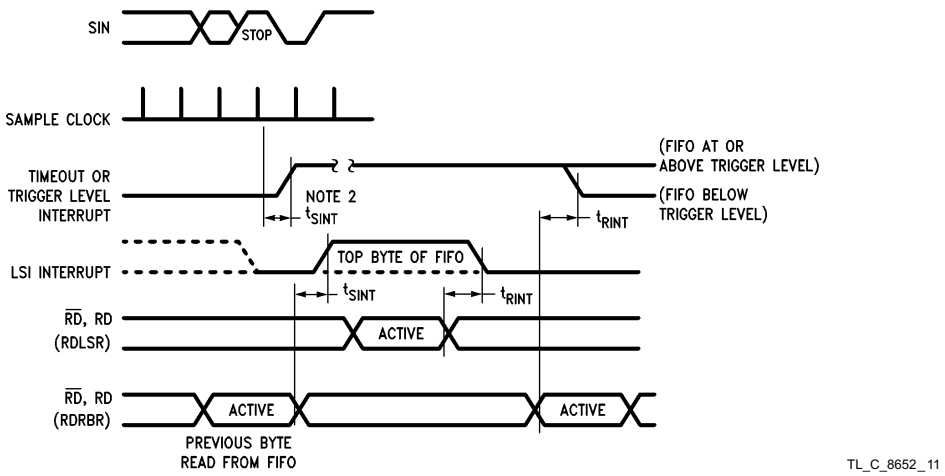
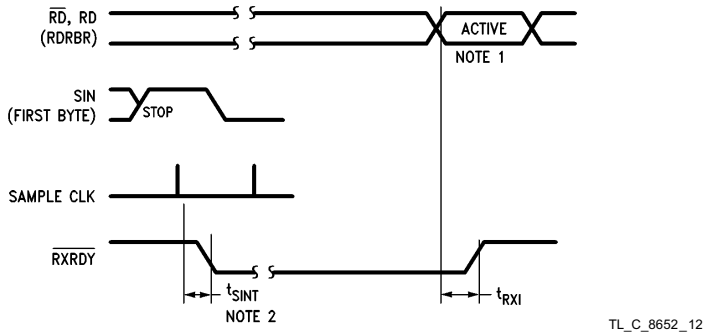


Figure 10. RCVR FIFO Bytes Other Than the First Byte (RDR is Already Set)

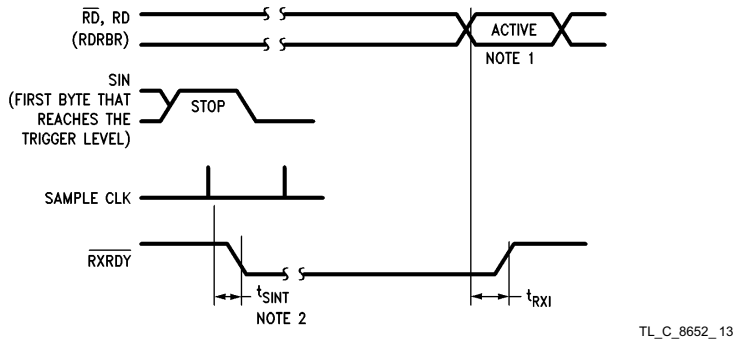


(1) This is the reading of the last byte in the FIFO.

(2) If FCR0 = 1, then t_{SINT} = 3 RCLKs. For a timeout interrupt, t_{SINT} = 8 RCLKs.

Figure 11. Receiver Ready (Pin 29) FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

All timings are referenced to valid 0 and valid 1.



(1) This is the reading of the last byte in the FIFO.

(2) If FCR0 = 1, t_{SINT} = 3 RCLKs.

Figure 12. Receiver Ready (Pin 29) FCR0=1 and FCR3=1 (Mode 1)

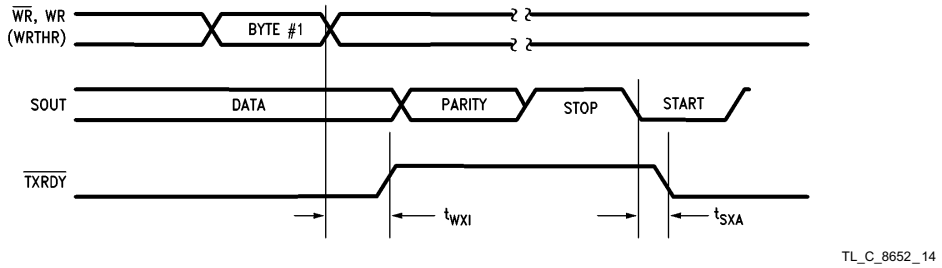


Figure 13. Transmitter Ready (Pin 24) FCR0=0 or FCR0=1 and FCR3=0 (Mode 0)

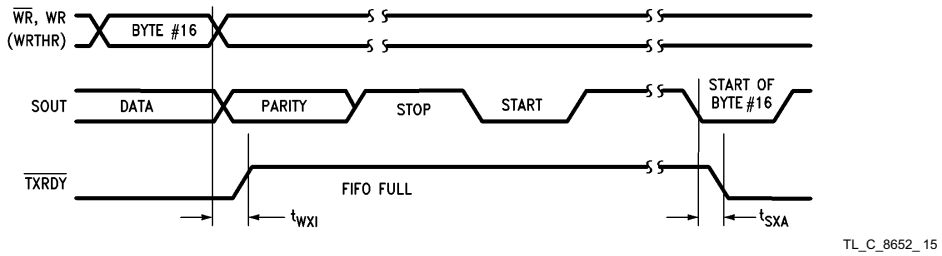


Figure 14. Transmitter Ready (Pin 24) FCR0=1 and FCR3=1 (Mode 1)

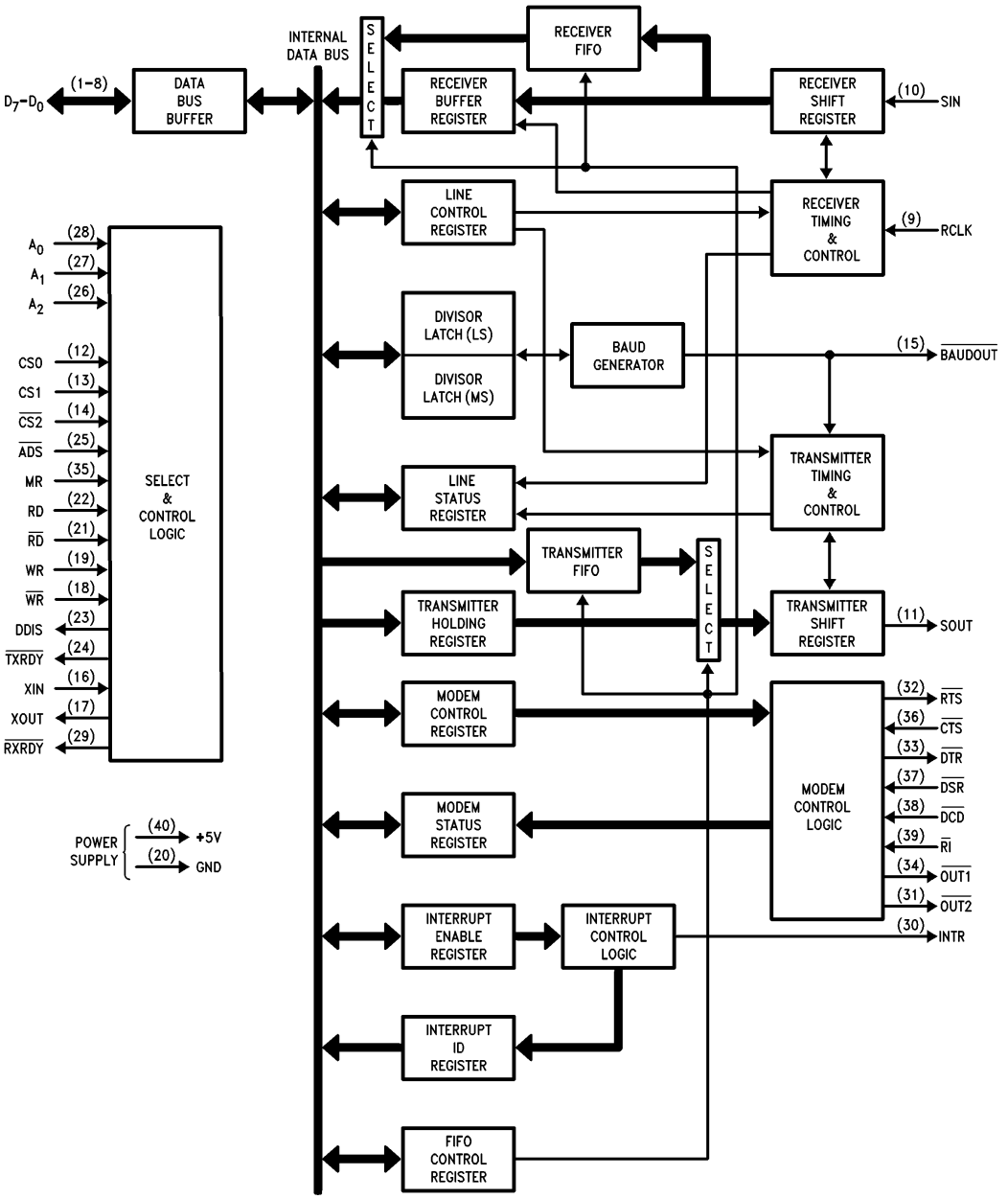
Copyright © 1995–2015, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The PC16550D is an improved version of the original 16450 Universal Asynchronous Receiver/Transmitter (UART). This device performs serilization/deserialization (ser/des) on data between a peripheral device, such as a modem, and the central processing unit (CPU). The PC16550D provides several status indicators to allow the cpu to monitor the type and status of data transfers.

8.2 Functional Block Diagram



NOTE: Applicable pinout numbers are included within parenthesis.

8.3 Feature Description

The PC16550D contains the full feature set and functionality of the 16450, but also features integrated transmit and receive FIFOs to relieve the CPU of excessive software overhead. Configuration of the modem status, modem control, interrupt enable, interrupt I/O, transmitter, receiver, line control registers are discussed in the *Registers* section. The PC16550D can be configured to support baud rates from DC to 1.5 M baud.

8.4 Device Functional Modes

8.4.1 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR0=1, IER0=1) RCVR interrupts will occur as follows

1. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.
4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

1. A FIFO timeout interrupt will occur, if the following conditions exist
   - at least one character is in the FIFO
   - the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
   - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

   The maximum time between a received character and a timeout interrupt will be 160 ms at 300 baud with a 12-bit receive character (that is, 1 Start, 8 Data, 1 Parity and 2 Stop Bits).
2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).
3. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
4. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0=1, IER1=1), XMIT interrupts will occur as follows:

1. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

8.4.2 FIFO Polled Mode Operation

With FCR0=1 resetting IER0, IER1, IER2, IER3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status through the LSR. As stated previously:

- LSR0 will be set as long as there is one byte in the RCVR FIFO.

Copyright © 1995–2015, Texas Instruments Incorporated

Device Functional Modes (continued)

- LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2=0.
- LSR5 will indicate when the XMIT FIFO is empty.
- LSR6 will indicate that both the XMIT FIFO and shift register are empty.
- LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

8.5 Programming

8.5.1 Programmable Baud Generator

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 24 MHz and dividing it by any divisor from 2 to 2^{16}–1. The output frequency of the Baud Generator is 16 × the Baud [divisor # = (frequency input) ÷ (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table 4 provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 18.432 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

8.6 Register Maps

Table 1. Summary of Registers

	REGISTER ADDRESS											
Bit No.	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0[1]	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) [2]	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled [2]	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14

(1) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
(2) These bits are always 0 in the 16450 Mode.

Copyright © 1995–2015, Texas Instruments Incorporated

Table 1. Summary of Registers (continued)

	REGISTER ADDRESS											
Bit No.	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled(2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO(2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

8.6.1 Registers

The system programmer may access any of the UART registers summarized in Table 1 through the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table 1 has its name and reset state shown.

Table 2. Register Addresses

DLAB	A_2	A_1	A_0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	0	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Copyright © 1995–2015, Texas Instruments Incorporated

Table 3. UART Reset Configuration

REGISTER/SIGNAL	RESET CONTROL	RESET STATE (1)
Interrupt Enable Register	Master Reset	**0000** 0000
Interrupt Identification Register	Master Reset	00**00** 0001
FIFO Control	Master Reset	00**00** 0000
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**0000** 0000
Line Status Register	Master Reset	0110 0000
MODEM Status Register	Master Reset	XXXX 0000 (2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High
RCVR FIFO	MR/FCR1●FCR0/DFCR0	All Bits Low
XMIT FIFO	MR/FCR1●FCR0/DFCR0	All Bits Low

(1) **Boldface** bits are permanently low.
(2) Bits 7 – 4 are driven by the input signals.

Table 4. Baud Rates, Divisors and Crystals

BAUD RATE	1.8432 MHz CRYSTAL		3.072 MHz CRYSTAL		18.432 MHz CRYSTAL	
	DECIMAL DIVISOR for 16 × Clock	PERCENT ERROR	DECIMAL DIVISOR for 16 × Clock	PERCENT ERROR	DECIMAL DIVISOR for 16 × Clock	PERCENT ERROR
50	2304	–	3840	–	23040	–
75	1536	–	2560	–	15360	–
110	1047	0.026	1745	0.026	10473	–
134.5	857	0.058	1428	0.034	8565	–
150	768	–	1280	–	7680	–
300	384	–	640	–	3840	–
600	192	–	320	–	1920	–
1200	96	–	160	–	920	–
1800	64	–	107	0.312	640	–
2000	58	0.69	96	–	576	–
2400	48	–	80	–	480	–
3600	32	–	53	0.628	320	–
4800	24	–	40	–	240	–
7200	16	–	27	1.23	160	–
9600	12	–	20	–	120	–
19200	6	–	10	–	60	–
38400	3	–	5	–	30	–
56000	2	2.86	–	–	21	2.04
128000	–	–	–	–	9	–

Copyright © 1995–2015, Texas Instruments Incorporated

8.6.2 Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and set the Divisor Latch Access bit through the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table 1 shows the contents of the LCR. Details on each bit follow.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected through bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

8.6.3 Line Status Register

This register provides status information to the CPU concerning the data transfer. Table 1 shows the contents of the Line Status Register. Details on each bit follow.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Copyright © 1995–2015, Texas Instruments Incorporated

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parityselect bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a logic 0 bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this ‘‘start’’ bit twice and then takes in the ‘‘data’’.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Table 5. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	–	None	None	–
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO During the Last 4 Char. Times and There Is at Least 1 Char. in It During This Time	Reading the Receiver
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Copyright © 1995–2015, Texas Instruments Incorporated

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concur- rently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Regis- ter (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the 16450 Mode this is a 0. In the FIFO mode LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

NOTE

The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing. In the FIFO mode the software must load a data byte in the Rx FIFO through Loopback Mode in order to write to LSR2–LSR4. LSR0 and LSR7 can't be written to in FIFO mode.

8.6.4 FIFO Control Register

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to en- able the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from the FIFO Mode to the 16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0=1 (see description of RXRDY and TXRDY pins).

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

8.6.5 Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table 1 shows the contents of the IIR. Details on each bit follow.

Copyright © 1995–2015, Texas Instruments Incorporated

Bit 0: This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5.

Bit 3: In the 16450 Mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5: These two bits of the IIR are always logic 0.

Bits 6 and 7: These two bits are set when FCR0=1.

8.6.6 Interrupt Enable Register

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the set- ting of the Line Status and MODEM Status Registers. Table 1 shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

8.6.7 Modem Control Register

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 1 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the loopback mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and received-data paths of the UART.

In the loopback mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

8.6.8 Modem Status Register

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 1 and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

8.6.9 Scratchpad Register

This 8-bit Read/Write Register does not control the UART in anyway. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Copyright © 1995–2015, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The PC16550D is a Universal Asynchronous Receiver/Transmitter (UART) with integrated transmit and receive FIFOs.

9.2 Typical Applications

The following sections describe the typical use cases and common implementation practices for this device.

9.2.1 Typical Interface for a High-Capacity Data Bus

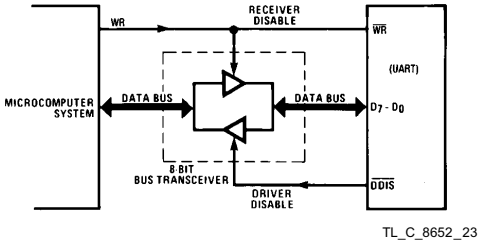


Figure 15. Typical Application Schematic

9.2.1.1 Design Requirements

This section lists some critical areas for printed circuit board design consideration and study.

- Be sure to provide adequate power supply decoupling and filtering. These components should be placed as close to the power pins as possible.
- Ensure that signals fed to the PC1550D do not violate datasheet input min and max specs. To avoid excursion (over-shoot, or under-shoot), consider implementing series termination resistors. These are typically on the order of 10 Ω to 33 Ω.

9.2.1.2 Detailed Design Procedure

To begin the design process determine the following:

- Maximum power draw for PCB regulator selection.
- Determine a clocking scheme for the baud rate generator. Either apply a system reference clock or implement a crystal based clock solution.
- Review datasheet descriptions for each register and plan for the desired device configuration and operating mode.

Copyright © 1995–2015, Texas Instruments Incorporated

Typical Applications (continued)

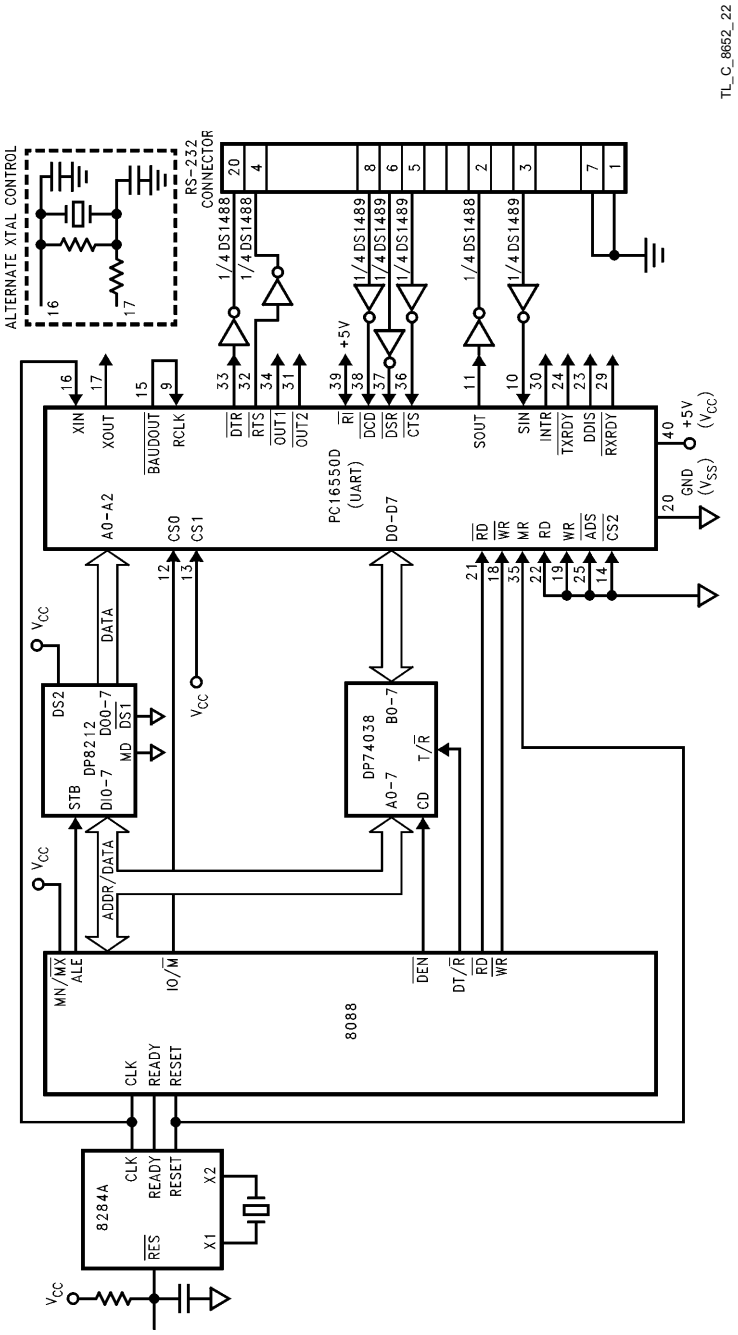
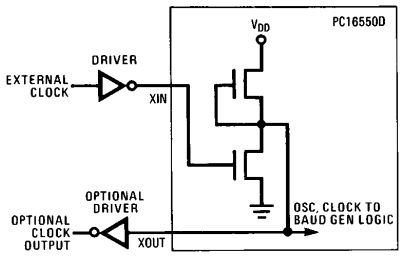


Figure 16. Basic Connections of an PC16550D to an 8088 CPU

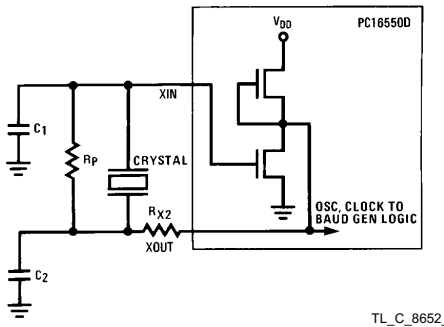
Copyright © 1995–2015, Texas Instruments Incorporated

9.3 System Examples

9.3.1 Typical Clock Circuits



TL_C_8652_19



TL_C_8652_20

Table 6. Typical Crystal Oscillator Network(1)

CRYSTAL	RP	RX2	C1	C2
3.1 MHz	1 MX	1.5k	10-30 pF	40-60 pF
1.8 MHz	1 MX	1.5k	10-30 pF	40-60 pF

(1) These R and C values are approximate and may vary 2x depending on the crystal characteristics. All crystal circuits should be designed specifically for the system.

10 Power Supply Recommendations

Power supply filtering typically consists of a bulk 22-µF capacitor with an array of 0.1-µF capacitors all placed near the device. Additional bypass capacitors or capacitors of different values may be required depending on system conditions.

11 Layout

11.1 Layout Guidelines

For a successful PCB layout, be sure to connect the power pins to power planes. Avoid long, skinny power traces. Route the parallel data lines and RCLK line as a phased match bus. Use controlled impedance traces for the serial data nets.

Copyright © 1995–2015, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 1995–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PC16550DN	NRND	PDIP	NFJ	40	9	TBD	Call TI	Call TI	0 to 70	PC16550DN PATENTED	
PC16550DN/NOPB	LIFEBUY	PDIP	NFJ	40	9	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	PC16550DN PATENTED	
PC16550DV	NRND	PLCC	FN	44	25	TBD	Call TI	Call TI	0 to 70	PC16550DV PATENTED	
PC16550DV/NOPB	ACTIVE	PLCC	FN	44	25	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 70	PC16550DV PATENTED	Samples
PC16550DVX	NRND	PLCC	FN	44	500	TBD	Call TI	Call TI	0 to 70	PC16550DV PATENTED	
PC16550DVX/NOPB	ACTIVE	PLCC	FN	44	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 70	PC16550DV PATENTED	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

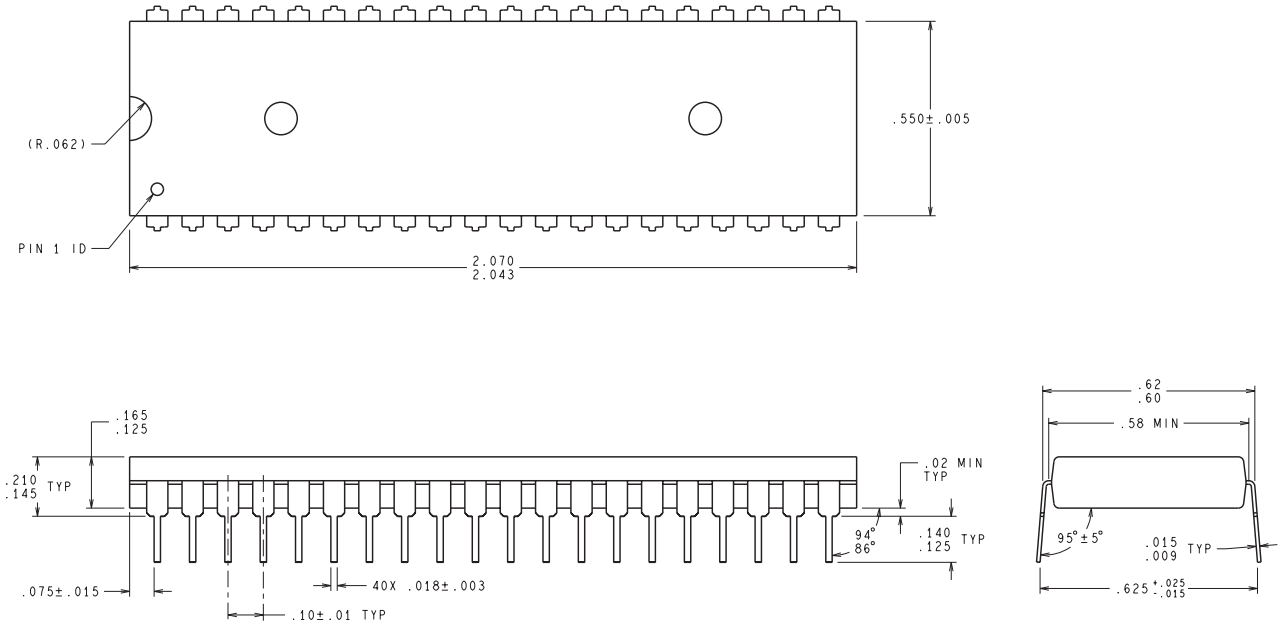
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

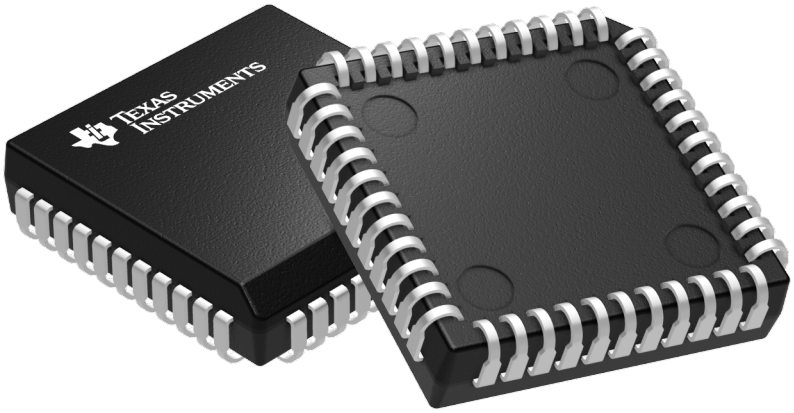
NFJ0040A



N40A (Rev E)

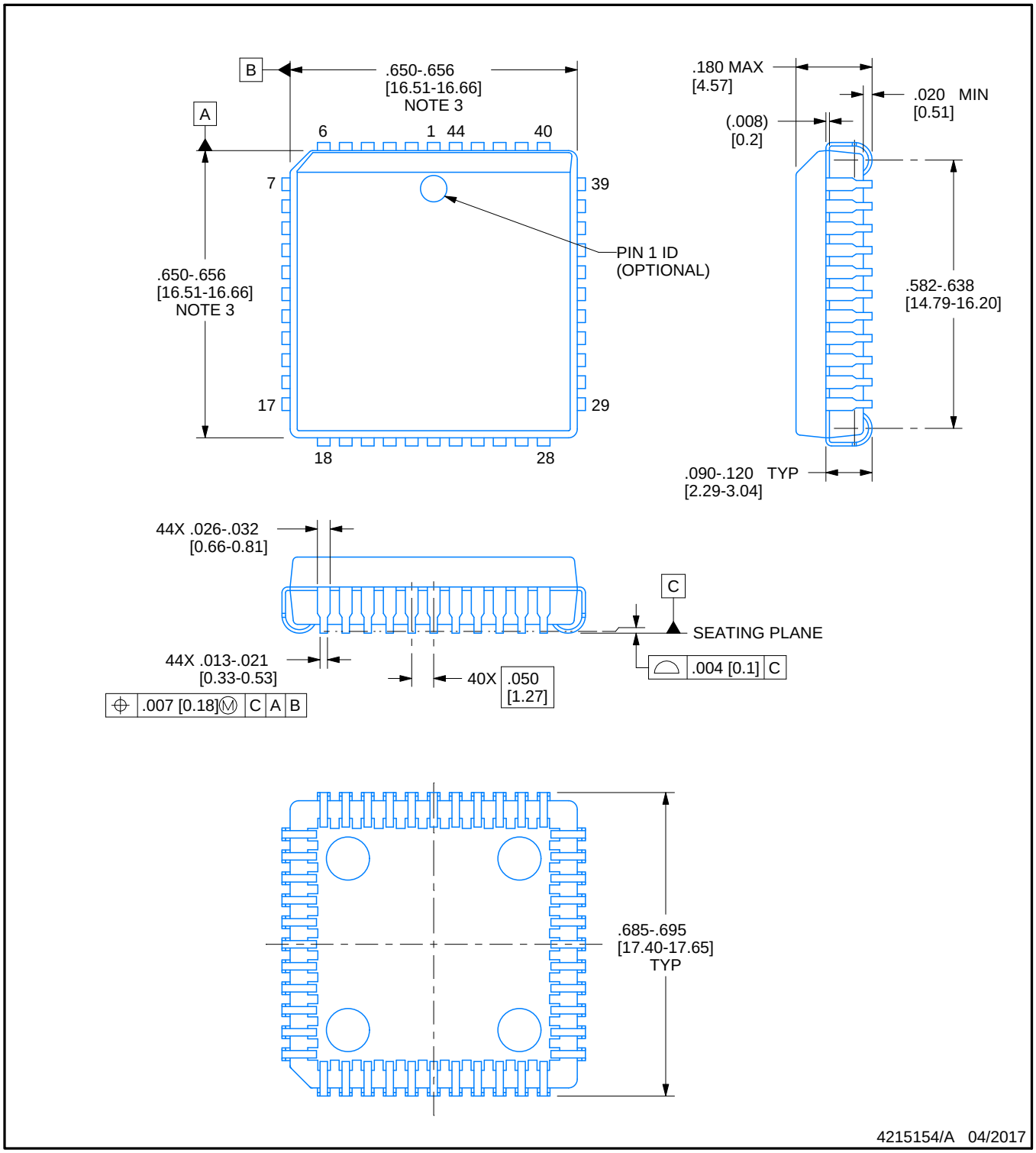
FN 44 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



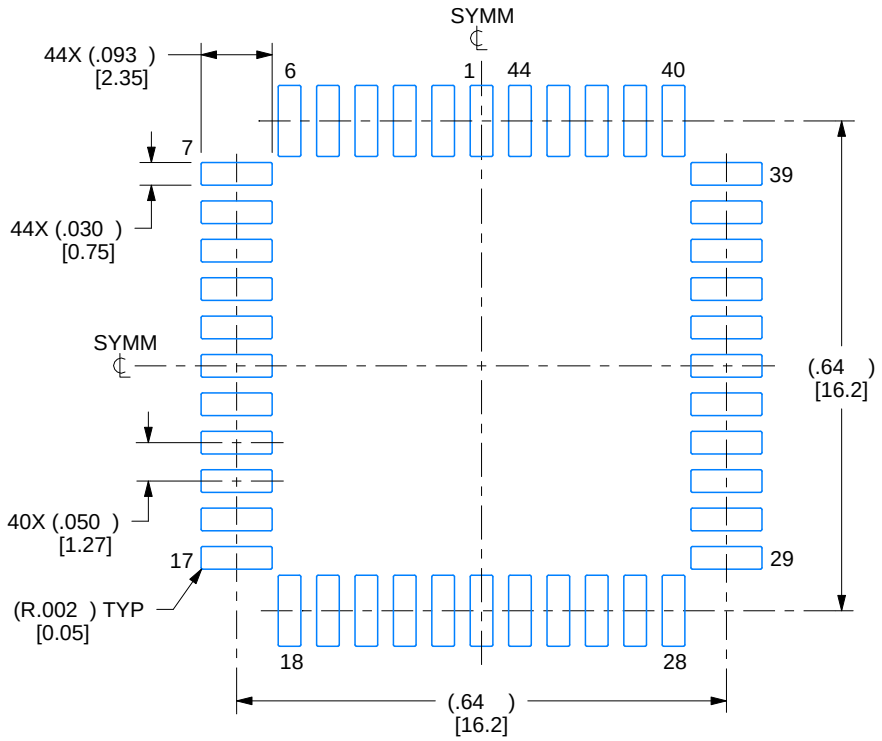
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040005-4/C

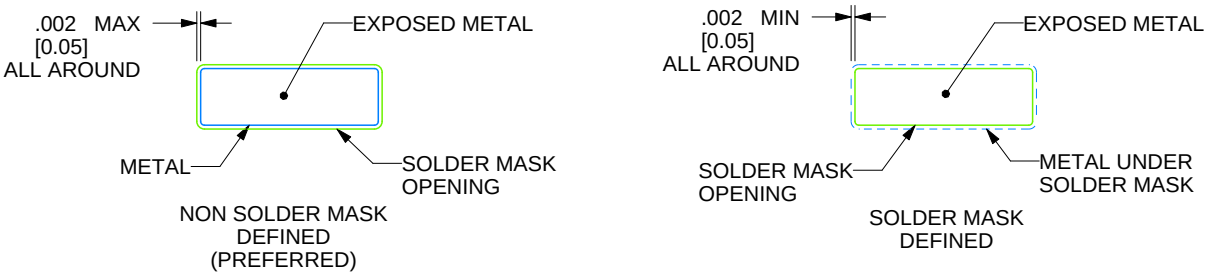


NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X

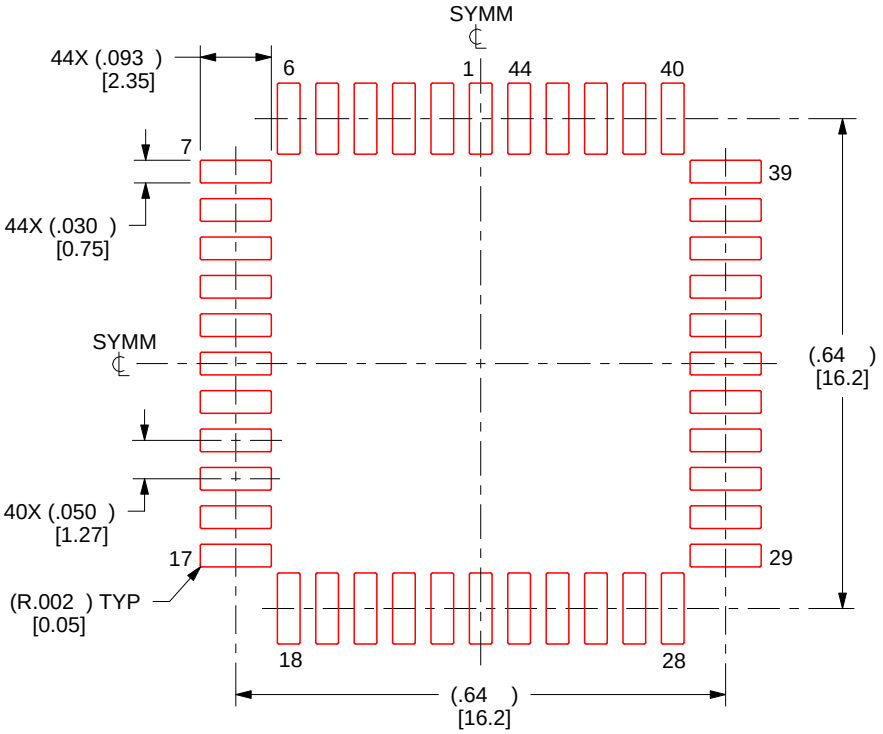


SOLDER MASK DETAILS

4215154/A 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4215154/A 04/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated